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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/696,897	10/29/2003	Sang-Hyun Lee	3364P146	9262

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BLAKELY SOKOLOFF TAYLOR & ZAFMAN
12400 WILSHIRE BOULEVARD
SEVENTH FLOOR
LOS ANGELES, CA 90025-1030

EXAMINER	
ABRAHAM, ESAW T	

ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 05/02/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/696,897	LEE ET AL.	
	Examiner	Art Unit	
	Esaw T. Abraham	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 and 2* is/are rejected.

7)☒ Claim(s) *3-10* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/29/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims **1-10** are presented for examination.

Priority

2. Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 119(a)-(d). The certified copy has been filed in parent Application No: 2002-83721 filed on 12/24/2002.

Information Disclosure Statement

3. The references listed in the information disclosure statement submitted on 10/29/03 have been considered by the examiner (see attached PTO-1449).

Specification

4. The specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham v. John Deere* CO., 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.

2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

5. Claims **1 and 2** are rejected under 35 U.S.C. 103(a) as being unpatentable over Richardson et al. (U.S. PN: 6,938,196).

As per claim 1:

Richardson et al. teach methods and apparatus for performing decoding operations that are used in conjunction with message passing decoding techniques and techniques and the techniques are suited for use with LDPC codes (see col. 1, lines 15-18) and to facilitate hardware implementation of an LDPC decoder, log-likelihood values are quantized to integer multiples of ½ In2 and further Circuitry for generating quantized log-likelihood values, e.g., ratios, from received values may be incorporated directly into a receiver which forms part of the communications channel 356 that precedes the message passing decoder (see figure 6 element 600) (see col. 6, lines 25-65 and col. 11, lines 43-58). Further, Richardson et al. teach means for generating log-likelihood values quantized to integer multiples of 1/2 ln 2 to produce quantized log-likelihood values coupled to a parity check decoder, for performing parity check decoding operations using said quantized log-likelihood values as input values (see claim 20) and furthermore the said parity check decoder includes variable node processing circuitry for performing a variable node processing operation using at least some of said produced quantized log-likelihood values; and check node processing circuitry (check node function unit) for performing a check node processing operation on quantized log-likelihood values produced by variable node processing (bit node

function unit) (see claims 20 and 21). Further, in figure 4, Richardson et al. teach LDPC code using a bipartite graph (400) wherein the graph includes m check nodes (constraint nodes) (402), n variable nodes (bit nodes) (406), and a plurality of edges (404). Messages between the check nodes and variable nodes (bit nodes) are exchanged over the edges (404). In addition, Richardson et al. teach that the sequence of performing processing at the variable nodes 406 comprising: transmitting generated messages to the check nodes (402), generating at the variable nodes soft outputs, and receiving messages from the check nodes, may be performed repeatedly, i.e., iteratively, until the outputs from the variable nodes (406) indicate that the codeword has been successfully decoded or some other stopping criterion, e.g., completion of a fixed number of message passing iterations, has been satisfied (see col. 8, lines 50-66 and col. 9, lines 11-28). Although Richardson et al. disclosed all the subject matter claimed in claim 1, it is noted however, Richardson et al. **did not explicitly** detail the aspect of parity-check (LPDC) message corresponding to an input from the bit node function unit calculated according to a linear approximation function as recited in claim 1. **However,** such linear approximation functions are common knowledge and known in the art of decoding LPDC since LPDC codes are basically linear block codes and the codes commonly comprise approximation functions. **Therefore,** it would have been obvious to a person having an ordinary skill in the art at the time the invention was made to employ a process according to a linear approximation for calculating bit node function. **This modification** would have been obvious because a person having ordinary skill in the art would have been motivated to do so because calculating bit

node function according to linear approximation is well known process of LPDC decoders.

As per claims 2:

Most of the limitations of these claims have been noted in the rejection of claim 1. In addition, Richardson et al. in figure 7 teach an implementation of a variable node processor (700) suitable for the decoder depicted in FIG. 6 and messages (m) for a particular variable node (bit node) arrive in sequence wherein each message, m, includes K bits and each received message is summed by the summer (710) with a previous sum, i.e., an accumulated message sum, output by unit delay element (712). The accumulated message sum supplied to summer (710) is reset to "0" with the receipt of a message corresponding to a new node (see col. 13, last paragraph and col. 14, lines 1-15). Further, Richardson et al. teach that if we choose delta. =1n2 then the computation required for the check node reliability update is particularly simple, allowing for an implementation using addition and shift operations (see col. 7, lines 37-64).

Claim objections

6. Claims **3-10** are objected to as being dependent upon a rejected base claim but would be allowable if rewritten independent from including all of the limitation of the base claim and any intervening claims.

a) The claimed invention comprises that the check node function comprises a slope calculator for calculating a slope to be multiplied from a bit of the highest order other than "0" in the input from the bit node function unit, and multiplying the slope with a bit shifter and a summator a boundary calculator for calculating a boundary value of

the linear approximation function for each interval from the bit of the highest order other than "0" in the input and a summator for adding the boundary value calculated by the boundary calculator to an output of the slope calculator (**as in claim 3**) which the prior art do not teach or render obvious.

Claims **4-5,** which are directly or indirectly dependents of claim 3 are also objected.

b) The claimed invention comprises that the logic function satisfies the equation as in claim 6 wherein x is the input from the bit node function unit (**as in claim 6**) which the prior art do not teach or render obvious.

Claims **7-10,** which are directly or indirectly dependents of claim 6 are also objected.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

US PN: 6,633,856 Richardson et al.

US PN: 7,013,116 Ashikhimin et al.

8. Any inquiry concerning this communication or earlier communication from the examiner should be directed to Esaw Abraham whose telephone number is (571) 272-3812. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are successful, the examiner's supervisor, Albert DeCady can be reached on (571) 272-3819. The fax phone numbers

for the organization where this application or proceeding is assigned are (571) 273-8300 for regular communications and (571) 273-8300 for after final communications.

Information regarding the status of an Application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or PUBLIC PAIR. Status information for unpublished applications is available through Private Pair only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Esaw Abraham

Art unit: 2133

ALBERT DECADY
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100